What is claimed is:

1. A method of manufacturing a semiconductor device comprising the steps of:

forming an impurity diffusion layer in a semiconductor substrate;

forming a first insulating film covering the semiconductor substrate;

forming a lower electrode of a capacitor on the first insulating film;

forming an oxide dielectric film of the capacitor on the lower electrode;

forming an upper electrode of the capacitor on the oxide dielectric film;

forming a second insulating film for covering the capacitor;

forming a first opening on or above the impurity diffusion layer and a second opening on the upper electrode in the first and second insulating films, by etching a part of the second insulating film and a part of the first insulating film;

forming an oxidation-preventing metal film on the second insulating film for connecting electrically the diffusion layer via the first opening and the upper electrode via the second opening;

forming a local interconnection in a range which pass through the first opening and the second opening and contains at least a region where the upper

electrode contacts the oxide dielectric film, by patterning the oxidation-preventing metal film; and

forming a third insulating film for covering the local interconnection.

2. A method of manufacturing a semiconductor device according to claim 1, wherein ~~the~~ an oxidation-preventing metal film constituting the local interconnection is formed of metal nitride.

3. A method of manufacturing a semiconductor device according to claim 2, wherein the metal nitride is one of titanium nitride, tungsten nitride or titanium-tungsten nitride.

4. A method of manufacturing a semiconductor device according to claim 1, wherein the step of forming the capacitor comprises the steps of,

setting the upper electrode into a size which defines a capacitor region by patterning the upper electrode,

leaving the oxide dielectric film at least below the upper electrode by patterning the oxide dielectric film, and

setting the lower electrode into a size which is wider than the oxide dielectric film by patterning the lower electrode.

5. A method of manufacturing a semiconductor device according to claim 1, wherein the step of forming the capacitor comprises the steps of,

patterning the oxide dielectric film and the lower electrode,

forming an intermediate insulating film for covering the oxide dielectric film and the lower electrode,

forming a window, which is employed to define ~~the~~ capacitor region, in the intermediate insulating film by patterning the intermediate insulating film, and

forming the upper electrode at least in the window.

6. A method of manufacturing a semiconductor device according to claim 1, wherein the second insulating film for covering the capacitor or the third insulating film is a silicon oxide film which is formed by using silane.

7. A method of manufacturing a semiconductor device according to claim 1, wherein the second insulating film is a silicon oxide film which is formed by using organic silicon compound source.

8. A method of manufacturing a semiconductor device according to claim 7, wherein the organic silicon compound source is tetra ethoxy silane.

9. A method of manufacturing a semiconductor device according to claim 1, wherein the oxide dielectric film is oxygen-annealed before and/or after the upper electrode of the capacitor is formed.

10. A method of manufacturing a semiconductor device according to claim 1, further comprising the

step of oxygen-annealing the oxide dielectric film via the second opening and the upper electrode after forming the second opening.

11. A method of manufacturing a semiconductor device according to claim 1, wherein the upper electrode is formed of a noble metal or a conductive ceramic which is not oxidized by ~~the~~ oxygen-annealing.

12. A method of manufacturing a semiconductor device according to claim 11, the noble metal is one of platinum, iridium or ruthenium.

13. A method of manufacturing a semiconductor device according to claim 1, wherein the oxide dielectric film is formed of PLZT, PZT, $(Ba,Sr)TiO_3$, $Pb(Zr,Ti)O_3$, $(Pb,La)(Zr,Ti)O_3$, $SrBi_2Ta_2O_9$ or Ta_2O_3.

14. A method of manufacturing a semiconductor device according to claim 1 further comprising the step of:

forming a conductive plug between the oxidation-preventing metal film and the diffusion layer in the first opening.

15. A method of manufacturing a semiconductor device according to claim 14, wherein the conductive plug is formed of tungsten.

16. A method of manufacturing a semiconductor device according to claim 1, wherein the impurity diffusion layer is a component part of an MOS transistor.

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17. A semiconductor device comprising:

an impurity diffusion layer formed on a semiconductor substrate;

a first insulating film for covering the impurity diffusion layer and a semiconductor substrate;

a capacitor formed on the first insulating film and consisting of a lower electrode, an oxide dielectric film, and an upper electrode;

a second insulating film for covering the capacitor;

first and second openings formed in the second insulating film to on or above the impurity diffusion layer and the upper electrode;

a local interconnection connected electrically with the impurity diffusion layer and the upper electrode respectively through the first and second openings and formed on the second insulating film in a range containing at least a region where the upper electrode contacts the oxide dielectric film; and

a third insulating film for covering the local interconnection.

18. A semiconductor device according to claim 17 further comprising,

a conducting plug formed between the impurity diffusion layer and the upper electrode in the first opening.

19. A semiconductor device according to claim 17,

wherein the local interconnection is composed of metal nitride.

20. A semiconductor device according to claim 19, wherein the metal nitride is one of titanium nitride, tungsten nitride or titanium-tungsten nitride.